



INTERNATIONAL TELECOMMUNICATION UNION

ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

G.811

(09/97)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA,
DIGITAL SYSTEMS AND NETWORKS

Digital transmission systems – Digital networks – Design
objectives for digital networks

**Timing characteristics of primary reference
clocks**

ITU-T Recommendation G.811

(Previously CCITT Recommendation)

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ITU-T RECOMMENDATION G.811

TIMING CHARACTERISTICS OF PRIMARY REFERENCE CLOCKS

Summary

This Recommendation outlines minimum requirements for timing devices used as primary reference clocks in synchronization networks. These networks include Public Switched Telephone Networks (PSTNs) and Synchronous Digital Hierarchy (SDH) networks.

Source

ITU-T Recommendation G.811 was revised by ITU-T Study Group 13 (1997-2000) and was approved under the WTSC Resolution No. 1 procedure on the 19th of September 1997.

Keywords

Clock, Clock Performance Objectives, Clock Performance Parameters, Jitter Performance, Wander Performance.

FOREWORD

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In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

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TIMING CHARACTERISTICS OF PRIMARY REFERENCE CLOCKS

(revised in 1997)

1 Scope

This Recommendation outlines the requirements for Primary Reference Clocks (PRCs) suitable for synchronization supply to digital networks. These requirements apply under the normal environmental conditions specified for digital equipment.

A typical PRC provides the reference signal for the timing or synchronization of other clocks within a network or section of a network. In particular, the PRC can also provide the reference signal to the slave clock specified in Recommendation G.812 within the network nodes where the PRC is located. This Recommendation defines the PRC output but it does not apply to the output of slave clock directly fed by a PRC. The long-term accuracy of the PRC should be maintained at 1 part in 10^{11} or better with verification to Coordinated Universal Time (UTC). A PRC may be realized as an autonomous clock, operating independently of other sources. Alternatively, the PRC may be realized as a non-autonomous clock which is disciplined by UTC-derived precision signals received from a radio or satellite system. In either case, the requirements for long-term accuracy and short-term stability, as specified in this Recommendation, apply.

The long-term accuracy of 1 part in 10^{11} or better is adequate when a single PRC provides the reference synchronization signal to all other clocks within a network (synchronous mode of operation). In the pseudo-synchronous mode, i.e. not all clocks in the network have timing traceable to the same PRC, the long-term accuracy is dependent on the number of PRCs in that network.

When more than one PRC is used in a network, a statistical approach is needed to determine the long-term accuracy of each PRC in that network.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published.

- [1] CCITT Recommendation G.703 (1991), *Physical/electrical characteristics of hierarchical digital interfaces*.
- [2] ITU-T Recommendation G.783 (1997), *Characteristics of Synchronous Digital Hierarchy (SDH) equipment functional blocks*.
- [3] ITU-T Recommendation G.810 (1996), *Definitions and terminology for synchronization networks*.
- [4] CCITT Recommendation G.812 (1988), *Timing requirements at the outputs of slave clocks suitable for pliesochronous operation of international digital links*.
- [5] CCITT Recommendation G.822 (1988), *Controlled slip rate objectives on an international digital connection*.
- [6] ITU-T Recommendation G.823 (1993), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy*.
- [7] ITU-T Recommendation G.824 (1993), *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy*.
- [8] ITU-T Recommendation G.825 (1993), *The control of jitter and wander within digital networks which are based on the Synchronous Digital Hierarchy (SDH)*.

3 Definitions

The terms and definitions used in this Recommendation are contained in Recommendation G.810.

4 Abbreviations

This Recommendation uses the following abbreviations:

CMI	Coded Mark Inversion
FPM	Flicker Phase Modulation
MTIE	Maximum Time Interval Error
NE	Network Element
OAM	Operations and Maintenance
PLL	Phase Locked Loop
PRC	Primary Reference Clock
SDH	Synchronous Digital Hierarchy
SEC	SDH Equipment Clock
SSMB	Synchronization Status Message Byte
STM	Synchronous Transport Module
TDEV	Time Deviation
UI	Unit Interval
UTC	Coordinated Universal Time
WFM	White Frequency Modulation

5 Frequency accuracy

The maximum allowable fractional frequency offset for observation times greater than one week is 1 part in 10^{11} , over all applicable operational conditions.

6 Noise generation

The noise generation of a PRC clock represents the amount of phase noise produced at its output. A suitable reference, for practical testing purposes, implies a performance level that is more stable than the output requirements. The ability of the clock to limit this noise is described by its frequency stability. The measures MTIE and Time Deviation (TDEV) are useful for characterization of noise generation performance.

MTIE and TDEV are measured through an equivalent 10 Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\tau$). For measurements over longer observation periods, alternative filter bandwidth and sampling time may be required for practical considerations.

6.1 Wander

The wander, expressed in MTIE, measured using the independent clock configuration defined in Figure 2a/G.810 should have the following limits:

$$\begin{array}{llll} \text{MTIE:} & 0.275 \times 10^{-3}\tau + 0.025 \mu\text{s} & \text{for} & 0.1 < \tau \leq 1000 \text{ s} \\ & 10^{-5}\tau + 0.29 \mu\text{s} & \text{for} & \tau > 1000 \text{ s} \end{array}$$

The resultant requirements are shown in Figure 1.

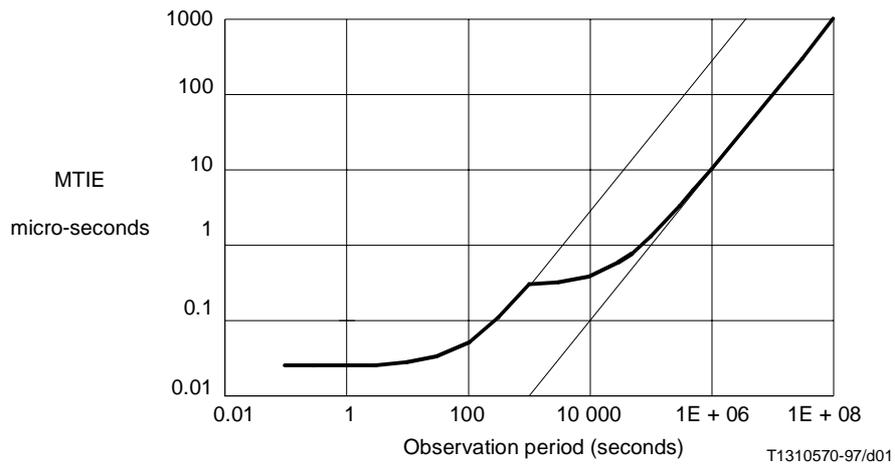


Figure 1/G.811 – MTIE as a function of an observation (integration) period τ

The wander, expressed in TDEV, measured using the independent clock configuration defined in Figure 2a/G.810 should have the following limits:

TDEV:	3 ns	for	$0.1 < \tau \leq 100$ s
	0.03τ ns	for	$100 < \tau \leq 1000$ s
	30 ns	for	$1000 < \tau < 10\,000$ s

The resultant requirements are shown in Figure 2.

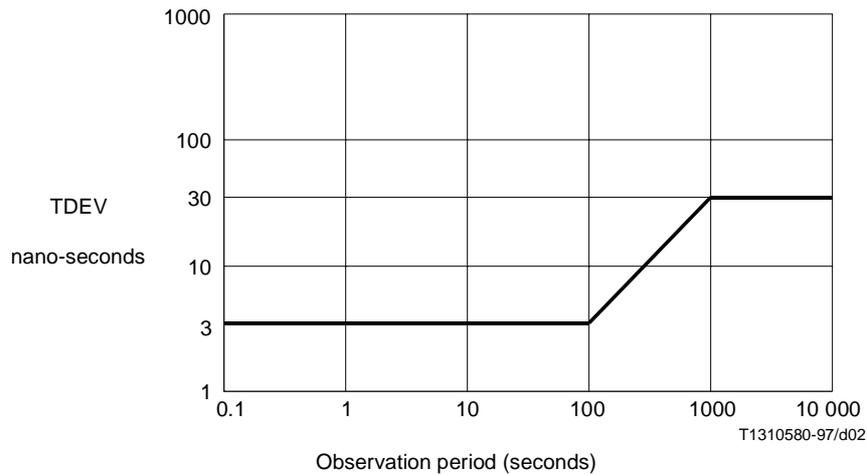


Figure 2/G.811 – TDEV as a function of an observation (integration) period τ

6.2 Jitter

While most specifications in this Recommendation are independent of the output interface at which they are measured, this is not the case for jitter production; jitter generation specifications must utilize existing specifications that are currently specified differently for different interface rates. These requirements are stated separately for the interfaces identified in clause 8. To be consistent with other jitter requirements, the specifications are in UIpp, where the UI corresponds to the reciprocal of the bit rate of the interface.

The intrinsic jitter at 2048 kHz and 2048 kbit/s output interfaces as measured over a 60-second interval shall not exceed 0.05 UIpp when measured through a single pole band-pass filter with corner frequencies at 20 Hz and 100 kHz.

The intrinsic jitter at 1544 kbit/s output interfaces as measured over a 60-second interval shall not exceed 0.015 UIpp when measured through a single pole band-pass filter with corner frequencies at 10 Hz and 40 kHz.

7 Phase discontinuity

Primary reference clocks need a very high reliability and are likely to include replication of the equipment in order to ensure the continuity of the output. However, any phase discontinuity, due to internal operations within the clock, should only result in a lengthening or shortening of the timing signal interval and must not, at the clock output, cause a phase discontinuity in excess of 1/8 UI (this refers to output signals at 1544 kbit/s, 2048 kbit/s or 2048 kHz).

8 Degradation of the performance of a PRC

If redundancy is applied and a clock frequency departs significantly from its nominal value, this should be detected and switching to an undegraded oscillator should then be effected. This switching should be accomplished before the MTIE or TDEV specification is exceeded.

9 Interfaces

The requirements in this Recommendation are related to reference points which may be internal to the equipment or NE in which the PRC is embedded and are therefore not necessarily available for measurement or analysis by the user. Consequently, the performance of the PRC is not specified at these internal reference points, but rather at the external interfaces of the equipment. The output interfaces specified for the equipment in which the PRC clock may be contained are:

- 2048 kHz interfaces according to clause 10/G.703 with additional jitter and wander requirements as specified herein;
- 1544 kbit/s interfaces according to clause 2/G.703 with additional jitter and wander requirements as specified herein;
- 2048 kbit/s interfaces according to clause 6/G.703 with additional jitter and wander requirements as specified herein;
- other interfaces (such as sine wave 8 kHz to 5 MHz) are for further study.

Note that not all of the above interfaces may be implemented on all equipment.

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